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In re Application of: §
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BENOUDIZ, Eyal §
§
Serial No.: 10/045,055 §
§
Filed: January 15, 2002 § Group Art Unit: 2133
§
For: System and Method for Visual Debugging § Attorney
of Constraint Systems § Docket: 24773
§ (Previously V02/16)
Examiner: §

INFORMATION DISCLOSURE STATEMENT

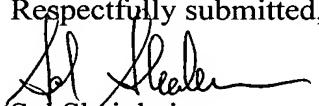
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Sir:

Enclosed is a PTO Form SB/08A which lists citations which may be material to the examination of the above identified application. Also enclosed are copies of the references cited. These are submitted in compliance with the duty of disclosure defined in 37 CFR 1.56. The Examiner is requested to make these citations of official record in this application.

This Information Disclosure Statement under 37 CFR 1.56 is not to be construed as a representation that a search has been made, that additional matter which is material to the examination of this application does not exist, or that any or more of these citations constitutes prior art.

Respectfully submitted,

Sol Sheinbein
Registration No. 25,457
Attorney for Applicant

Date: September 17, 2002



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PTO/SB/08A (10-96)

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| Sheet | 1 | of | 1 | Attorney Docket Number | 24773 Previously V02/16 |
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U.S. PATENT DOCUMENTS

| Examiners Initials | Cite No. ¹ | U.S. Patent Document | | Name of Patentee or Applicant of Cited Document | Date of Publication of Cited Document MM-DD-YYYY | Pages, columns, lines, Where Relevant Passages or Relevant Figures Appear |
|--------------------|-----------------------|----------------------|--------------------------------------|---|---|--|
| | | Number | Kind Code ² (if known) | | | |
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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

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| Examiner Initials | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published. | T ² |
| | AG | Benjamin et al, A Study in Coverage-Driven Test Generation, DAC, 1999, pp. 970 – 975 | |
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| | AK | Greggian et al, Fault Grading, A Measure of Logic Simulation Integrity, Proc. 2 nd Annual IEEE ASIC Seminar and Exhibit, 1989, pp 9-2.1 – 9-2.4 | |
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